REMARKS

Claims 2-8, 10-14, 17 and 19 remain in the application. Applicant asserts that no new matter has been added. Reconsideration of the Application is hereby requested.

Claim Rejections

Rejections Under 35 U.S.C. § 102

Claims 2, 3, 6, 10, 11, 14, 17 and 19 were rejected under 35 U.S.C. § 102(b), as being anticipated by Chiarot.

In the Office Action dated 10/14/2008, the Examiner asserted that Chiarot discloses the limitations of "at least one fast-load data cache that loads at least one speculative data load relative to the speculative instruction into the pipeline," as recited in Claim 17, and "loading a non-speculative load into the pipeline a predetermined number of cycles after the action of loading a speculative load," as recited in Claim 19. (Office Action, p. 6) However, Chiarot simply fails to disclose these limitations.

In its "Background of the Invention" section, cited in the Action, Chiarot states "...design techniques of speculative execution, deeper pipelines, more execution elements and the like, continue to improve the performance of processing systems." (Chiarot, col. 1, ll. 33-36) Later, Chiarot sates "[t]o increase the performance of processing systems, cache memory systems are often implemented." (Chiarot, col. 1, ll. 38-40) The only reasonable way to read this passage is it is stating that the prior art employs several methods to improve processor performance, including "cache memory systems" and "deeper pipelines." One simply cannot conclude that this passage discloses a cache memory system used in a pipeline, much less a system in which both a speculative load and a non-speculative load are loaded into a pipeline, as recited in the claims of the present application. There is simply no connection made by Chiarot between a pipelined system and a cache memory system.

The key to a pipelined architecture is simultaneous execution of a plurality of instructions via a corresponding plurality of processing units (*e.g.*, processors or arithmetic logic units). This is clearly demonstrated in Exhibit C, attached hereto, which is the section entitled Pipeline Computers from Hwang et al., Computer Architecture and Parallel Processing, Mcgraw-Hill Book Company, 1984, pp. 20-22, which has been one of the authoritative texts for graduate-level courses in advanced computer architecture for twenty-five years. It clearly shows that pipelined execution involves simultaneous execution of instructions. *See, also*, Exhibit D, Anderson et al., "The IBM System/360 Model 91: Floating-Point Execution Unit," IBM Journal, Jan. 1967, pp. 34-53 (which shows that this conception of pipelined architecture has been generally accepted since the early days of computing). This definition of pipelined computer architectures has also been long recognized by the Patent Office (*See, e.g.,* U.S. Patent Nos. 3,728,692; 4,057,846 and 4,858,113)

Chiarot makes no disclosure of loading anything into a pipeline and it makes no disclosure of anything that executes a plurality of instructions simultaneously. It merely discloses a method for prefetching instructions into an L1 instruction cache from an L2 cache. It certainly fails to disclose the loading of both a speculative load into a pipeline and then loading a non-speculative load into the pipeline a predetermined number of cycles later, as recited in the rejected claims. While it is conceivable that the cache used in Chiarot might be used in a pipelined system (even though Chiarot clearly does not make that disclosure), there is no indication that two types of loads (speculative and non-speculative) would both be loaded into such a pipeline. Therefore, Chiarot simply does not disclose the recited limitations.

For this reason, Applicant believes that this rejection has been overcome and respectfully requests that it be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 4, 5, 12 and 13 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Chiarot et al. in view of Au.

As asserted above, Chiarot fails to disclose elements recited in the claims from which the claims rejected under §103 depend. Au does not disclose these limitations and no combination of Chiarot and Au would teach or fairly suggest these limitations.

For this reason, Applicant believes that this rejection has been overcome and respectfully requests that it be withdrawn.

Request for specific findings of fact in anticipation of the filing of a Notice of Appeal

Based on the record, it appears as though there might be a fundamental disagreement between the Examiner and the Applicant regarding the nature of Chiarot, which may be resolvable only through the filing of an Appeal. Therefore, to mature the record for Appeal, Applicant respectfully request that the Examiner provide specific answers to the following questions in the next action if the pending claims are not allowed:

1. If the Examiner maintains that Chiarot discloses the loading of a speculative load into a pipeline, indicate exactly which column and line number in Chiarot shows a pipeline in which a speculative load is being loaded.
2. If the Examiner maintains that Chiarot discloses the loading of a non-speculative load into the pipeline a predetermined number of cycles after the loading of the speculative load, indicate exactly which column and line number in Chiarot shows a pipeline in which a non-speculative load is being loaded.
3. Further pursuant to question 2., indicate exactly where Chiarot discloses the separation of a predetermined number of cycles between the loading of the speculative load and the non-speculative load.
4. If the Examiner maintains that Chiarot discloses an instruction that includes a flag, indicate exactly which paragraph or figure in Chiarot shows a flagged instruction.

CONCLUSION

Applicant believes that the rejections have been overcome for the reasons recited above. Therefore, Applicant respectfully requests that all remaining claims be allowed and that a timely Notice of Allowance be issued.

No addition fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees that may be required, including any necessary extensions of time, which are hereby requested, to Deposit Account No. 503535.

01/14/2009
Date

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